a plurality of signal lines for connecting the macro circuits to one another into a loop to transmit signals in a single specified direction through the signal lines in synchronization with a clock signal,

each of the macro circuits receiving the signals at the input terminals thereof, accepting the received signals if the received signals are destined thereto, and transferring the received signals to the output terminals thereof without accepting the received signals if the received signals are not destined thereto.

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17. (Amended) An electronic circuit system comprising:

a first macro circuit constituted by a logic circuit having a plurality of input terminals and a plurality of output terminals;

second to "n"th macro circuits (n being an integer larger than 3) each including a memory circuit but no logic circuit, and having a plurality of input terminals and a plurality of output terminals; and

a plurality of signal lines for connecting the first to "n"th macro circuits to one another into a half loop with the output terminals of the first macro circuit being at the start of the half loop and the input terminals of the first macro circuit at the end of the half loop, to transmit signals in a single specified direction through the signal lines in synchronization with a clock signal,

the first macro circuit accepting signals received by the input terminals thereof if the received signals are destined for the first macro circuit,

each of the second to "n"th macro circuits accepting signals received by the input terminals thereof if the received signals are destined thereto and transmitting the

received signals as they are from the output terminals thereof, without accepting the received signals, if the received signals are not destined thereto.

29. (Amended) An electronic circuit system comprising:

a plurality of external input terminals for receiving test signals;

first to "m-1"th macro circuits (m being an integer larger than 2) each having a plurality of input terminals and a plurality of output terminals for receiving and transmitting the test signals;

an "m"th macro circuit having input terminals for receiving the test signals; and

a plurality of signal lines for transmitting the test signals and connecting the external input terminals and the first to "m"th macro circuits to one another into a half loop with the external input terminals being at the start of the half loop and the input terminals of the "m"th macro circuit at the end of the half loop, to transmit the test signals in single specified direction through the signal lines in synchronization with a clock signal,

each of the first to "m-1"th macro circuits accepting the test signals received by the input terminals thereof if the test signals are destined thereto.

the "m"th macro circuit accepting the test signals received by the input terminals thereof if the test signals are destined thereto.

34. (Amended) A signal transmission method comprising the steps of:

connecting at least three macro circuits each having a plurality of input terminals and a plurality of output terminals to one another into a loop to transmit signals in a single specified direction through signal lines in synchronization with a clock signal; and

making each of the macro circuit accept signals received by the input terminals thereof if the received signals are destined thereto and transfer the received signals as they are, without accepting them, to the output terminals thereof if the received signals are not destined thereto.

35. (Amended) A signal transmission method comprising the steps of:

connecting first to "n"th macro circuits (n being an integer larger than 3) each having a plurality of input terminals and a plurality of output terminals to one another through signal lines into a half loop, the first macro circuit being a logic circuit, each of the second to "n"th macro circuits including a memory circuit but no logic circuit and having a plurality of input terminals and a plurality of output terminals, the output terminals of the first macro circuit being at the start of the half loop, the input terminals of the first macro circuit being at the end of the half loop to transmit signals in a single specified direction through the signal lines in synchronization with a clock signal;

making each of the second to "n"th macro circuits accept signals received by the input terminals thereof if the received signals are destined thereto and transmit the received signals are destined thereto and transmit the received signals from the output terminals thereof, without accepting the received signals, if the received signals are not destined thereto; and

making the first macro circuit accept signals received by the input terminals thereof if the received signals are destined thereto.

36. (Amended) A signal transmission method comprising the steps of:

connecting a plurality of external input terminals for receiving test signals, first to "m-1"th macro circuits (m being an integer greater than 2) each having a plurality of input terminals and a plurality of input terminals for receiving and transmitting the test signals, and an "m"th macro circuit having a plurality of input terminals for receiving the test signals, to one another into a half loop through signals lines for transmitting the test signals, the external input terminals being at the start of the half loop, the input terminals of the "m"th macro circuit being at the end of the half loop to transmit the test signals in a single specified direction through the signal lines in synchronization with a clock signal;

making each of the first to "m"th macro circuits accept the test signals received by the input terminals thereof if the test signals are destined thereof and transmitting the test signals from the output terminals thereof, without accepting the test signals, if the test signals are destined thereto; and

making the "m"th macro circuit accept the test signals received by the input terminals thereof if the test signals are destined thereto.

REMARKS

The Office Action dated July 18, 2001 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete